In the Specification

(a) On page 2, please replace the paragraph beginning at line 1 by the following:

In one embodiment, the rotator in the phase-locked loop provides that the first (Q) and second (I) periodic signals are given by the equations:

$$Q=A\ cos(kf(p))$$

$$I=A\ sin(kf(p))$$

where A is the amplitude of the Q and I signals, k is a gain of the rotator circuit, and $f(p)$ representing a function of the phase difference. In one instance, the phase difference is represented in the phase signal as a voltage. The third and fourth periodic signals may each have a frequency that is substantially a frequency of the input signal. The rotator may further include an enforcer providing an error signal indicating a deviation in amplitude of the first and second periodic signals. This error signal is fed back to the rotator to maintain a substantially constant amplitude in the Q and I signals. In one instance, the error signal is a function of the value $\Delta = r^2 - I^2 - Q^2$, where r is a desired amplitude for the Q and I signals. In one implementation, the desired amplitude is approximately 0.4 volts.

(b) On page 9, please replace the paragraph beginning at line 27 as follows:

FIG. 7 shows enforcer circuit 1100, which can be used to implement enforcer 707 of FIG. [8] 4, in accordance with one embodiment of the present invention. As shown in FIG. 7, enforcer circuit 1100 includes differential multipliers 1101-1003, and resistors 1104-1107 and NMOS transistor 1108. Differential multipliers 1101-1103 can each be implemented, for example, by differential multiplier circuit 900 of FIG. 5. Multipliers 1101 and 1102 are configured to compute the squares of signals 113 and 114 (i.e., $I^2(t)$ and $Q^2(t)$), respectively. Transistor 1108 is biased by input bias signal at terminal 1120. In conjunction with resistors 1104-1105, transistor 1108 provides a current that is approximately 200 uA, thus providing a 0.4 volts differential input signal to

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multiplier 1103. 0.4 volts correspond to approximately twice the peak amplitude of the AC components of input signals 113 and 114. The output terminals of multipliers 1101-1103 are configured to provide output differential signal 708, which is the output differential signal of multiplier 1103, less the sum of the output differential signals of multipliers 1101-1102. (The polarity of the output differential signal of multiplier 1101 and 1102 are reversed.) Thus, output differential signal 708 (i.e., signal Δ) represents the value $\Delta = r^2 - I^2 - Q^2$.

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